Docket No. 0756-1974

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:	)	Group Art Unit: 2822
Yasuhiko TAKEMURA et al.	)	Examiner: M. Wilczewski
Serial No. 09/321,715	)	
Filed: May 28, 1999	)	
For: SEMICONDUCTOR DEVICE AND PROCESS FOR FABRICATING THE SAME	)	

CERTIFICATE OF MAILING

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Adela M Stampu

APPEAL BRIEF

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the provisions of 35 U.S.C. § 134 and 37 C.F.R. § 1.192(a), Appellants submit this Appeal Brief in triplicate to appeal the examiner's final rejection of claims 1, 3-9, 11-17, 19-25, 27-33, 35-41 and 43-117 in the Official Action mailed April 4, 2003, and the Advisory Action mailed September 11, 2003.

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I. REAL PARTY IN INTEREST

The named inventors have assigned all ownership rights in the pending application to Semiconductor Energy Laboratory Co., Ltd., 398, Hase, Atsugi-shi, Kanagawa-ken, 243-0036, Japan, which is the real party in interest.

II. RELATED APPEALS AND INTERFERENCES

The appellants, their legal representatives, and the assignee are not aware of any other pending appeals or interferences which will directly affect or be directly affected by, or have a bearing on the Board's decision in this appeal.

III. STATUS OF THE CLAIMS

Claims 1, 3-9, 11-17, 19-25, 27-33, 35-41 and 43-117 are pending in the present application, of which claims 1, 9, 17, 25, 33, 41, 49, 56, 63, 70, 78 and 86 are independent. No claims have been deemed allowable by the examiner.

IV. STATUS OF AMENDMENTS

All prior amendments are believed to have been entered in the present application. Thus, the status of the claims in this application is as set forth above and in Appendix A.

V. SUMMARY OF THE INVENTION

The present invention relates to a method of manufacturing a semiconductor device having a plurality of thin film transistors, comprising the steps of forming a semiconductor film (*e.g.* silicon film 12, 33, 44 or 58) comprising silicon either over a glass substrate (*e.g.* substrate 10, 31, 42 or 56), on an insulating surface (*e.g.* base film 11, 32, 43 or 57), or over an alkali-free glass substrate (*e.g.* an alkali-free borosilicate glass such as Corning 7059 glass); crystallizing the semiconductor film (*e.g.* page 9, lines 16-18; page 14, lines 13-15; page 19, line 15, to page 20, line 4; page 25, line 11, to page 26, line 1); and oxidizing the crystallized semiconductor film to be active layers of the thin film transistors in a pressurized atmosphere, for example, at a pressure greater than one atmosphere up to 15 atmospheres (*e.g.* page 5, lines 12-14; page 9, line 18, to page 10, line 4; page 14, line 15, to page 15, line 1; page 20, lines 5-8; page 26, lines 2-15), either

at a temperature lower than a strain point of the glass substrate, or at a temperature of 500 to 650°C (*e.g.* page 4, lines 7-16; page 9, line 18, to page 10, line 9; page 14, line 15, to page 15, line 4; page 20, lines 5-12; page 26, lines 2-14).

The method may further comprise one or more of the following features: forming an insulating film adjacent to the crystallized semiconductor film, which may be performed by plasma CVD (*e.g.* insulating film 16; oxide films 37a, 37b; silicon oxide film 51; silicon oxide film 65); forming gate electrodes adjacent to the insulating film (*e.g.* gate electrodes 17n, 17p, 17c; 38n, 38p, 38c; 52n, 52p, 52c; 66); and oxidizing the crystallized semiconductor film for electrically isolating the plurality of thin film transistors from one another (*e.g.* page 4, lines 7-10).

VI. STATEMENT OF ISSUES

A. Whether claims 1-117 are not *prima facie* obvious based on the combination of U.S. Patent No. 5,322,807 to Chen et al. and U.S. Patent No. 4,597,160 to Ipri, either alone or in combination with one or more of the following references: U.S. Patent No. 4,851,363 to Troxell et al., Wolf et al., "Silicon Processing for the VLSI Era, Volume 1: Process Technology," 1986, pp. 171-175 (Wolf I) and 216-218 (Wolf II).

B. Whether claims 1-105 do not conflict with claims 1, 2, 12, 13, 17 and 18 of copending Application No. 09/222,185, and with claims 1 and 6 of copending Application No. 09/615,078; and whether claims 1-105 are patentable under the doctrine of obviousness-type double patenting over claims 1-26 of the '185 application in view of U.S. Patent No. 5,275,851 to Fonash et al., and over claims 1-44 of the '078 application in view of Fonash.

VII. GROUPING OF CLAIMS

The rejected claims shall stand or fall together.

VIII. ARGUMENTS

A. Whether claims 1-117 are not *prima facie* obvious based on the combination of U.S. Patent No. 5,322,807 to Chen et al. and U.S. Patent No. 4,597,160 to Ipri, either alone or in combination with one or more of the following references: U.S. Patent No. 4,851,363 to Troxell et al., Wolf et al., "Silicon Processing for the VLSI Era, Volume 1: Process Technology," 1986, pp. 171-175 (Wolf I) and 216-218 (Wolf II).

The Official Action rejects claims 1-117 as obvious based on the combination of U.S. Patent No. 5,322,807 to Chen et al. and U.S. Patent No. 4,597,160 to Ipri, either alone or in combination with one or more of the following references: U.S. Patent No. 4,851,363 to Troxell et al., Wolf et al., "Silicon Processing for the VLSI Era, Volume 1: Process Technology," 1986, pp. 171-175 (Wolf I) and 216-218 (Wolf II). Specifically, the Official Action rejects claims 1-12, 14-16, 49-58, 60-62, 70-81, 83-85, 94, 106, 107, 112, 113, 115 and 116 as obvious based on the combination of Chen and Ipri; claims 17-24, 63-69, 86-93, 95, 108, 114 and 117 based on the combination of Chen, Ipri and Troxell; dependent claims 13, 59, 82, 98, 102 and 104 based on the combination of Chen, Ipri and Wolf II; dependent claims 99, 103 and 105 based on the combination of Chen, Ipri, Troxell and Wolf II; claims 25-36, 38-40, 96, 109 and 110 based on the combination of Chen, Ipri and Wolf I; claims 41-48, 97 and 111 based on the combination of Chen, Ipri, Wolf I and Troxell; dependent claims 37 and 100 based on the combination of Chen, Ipri, Wolf I and Wolf II; and dependent claim 101 based on the combination of Chen, Ipri, Wolf I, Troxell and Wolf II. The Applicants respectfully traverse the rejection because the Official Action has not made a *prima facie* case of obviousness.

As stated in MPEP §§ 2142-2143.01, to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. Obviousness can only be established by combining or modifying the

teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art. "The test for an implicit showing is what the combined teachings, knowledge of one of ordinary skill in the art, and the nature of the problem to be solved as a whole would have suggested to those of ordinary skill in the art." *In re Kotzab*, 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000). *See also In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). Once a *prima facie* case of obviousness has been made by the Patent Office, the burden then shifts to Applicant to rebut that *prima facie* case. This rebuttal can include any arguments or presentation of evidence that is pertinent to the issue of unobviousness including, for example, that the prior art is so deficient that there is no motivation to make what might appear to be obvious changes. See *In re Dillon*, 16 U.S.P.Q.2d 1897, 1901 (Fed. Cir. 1990); MPEP § 2142.

Also, MPEP § 2142 states that the examiner bears the initial burden of factually supporting any *prima facie* conclusion of obviousness. It is respectfully submitted that the Official Action has failed to carry this burden. While the Official Action relies on various teachings of the cited prior art to disclose aspects of the claimed invention and asserts that these aspects could be used together, it is submitted that the Official Action does not adequately set forth why one of skill in the art would combine the references to achieve the present invention.

Chen appears to teach a silicon region 3 having source/drain regions 5 and channel region 7, and a gate structure 9 having oxide region 11 and conducting region 13 separated from the silicon 3 (column 3, lines 11-29), recrystallization after deposition (*Id.* at line 42), and forming an oxide layer 11 which is a composite structure having a third layer 111, a grown layer 113 (also referred to as a first layer 113), and an optional deposited layer 115 (column 3, line 55, to column 4, line 38). The optional desposited layer 115 may be a TEOS SiO_2 layer that is densified by high-pressure oxidation (HiPOX) (column 3, line 59). The grown layer "can be grown thermally at a temperature less than 825°C or by HiPOX" (*Id.* at line 65). The third layer may be "grown underneath the first layer [113] by an oxidizing HiPOX anneal at a pressure between 1

and 10 atmospheres and a temperature less than 825°C" (column 4, line 21). It is noted that Chen only discusses a TEOS SiO_2 layer 115 that is densified by HiPOX, a grown/first layer 113 which can be grown by HiPOX, or a third layer 111 which can be grown underneath the first layer by an oxidizing HiPOX anneal.

However, Chen does not teach or suggest oxidizing a crystallized semiconductor film in a pressurized atmosphere. Specifically, Chen does not teach or suggest oxidizing the silicon region 3 in a pressurized atmosphere or applying the HiPOX process for layers 111, 113 or 115 to the silicon region 3. Also, the Official Action concedes that "Chen does not specifically teach to use temperatures in a range of 500 to 650°C, or temperatures below the strain point of the glass substrate" (page 3, Paper No. 30). Therefore, Chen does not teach or suggest oxidizing a crystallized semiconductor film to be active layers of a thin film transistor in a pressurized atmosphere at a temperature lower than a strain point of a glass substrate or at a temperature of 500 to 650°C.

Ipri appears to teach depositing an active layer 14 "using low pressure chemical vapor deposition (LPCVD) ... at a substrate temperature of about 550°C to 570°C" (column 2, lines 3-8), and "heating the active layer 14 at or slightly below T_c [about 620°C] in an oxidizing ambient, in particular heating to between about 580°C and 620°C, in a 100 percent steam ambient to grow a 60 nm thick insulating layer 23 at 600°C" (*Id.* at lines 21-26). Ipri also teaches "an insulating layer grown at 600°C for 120 hours in a steam ambient at one atmosphere" (column 2, line 67, to column 3, line 1). Ipri does not teach or suggest a pressurized atmosphere. Also, Ipri does not teach or suggest a strain point of a glass substrate.

There is no suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify Chen and Ipri or to combine reference teachings to achieve the claimed invention.

The Official Action asserts that "it would have been obvious to one skilled in the art that the oxidation temperatures of Ipri could have been used in the known method of Chen et al., since these temperatures are below 825°C" and "that the oxidizing atmosphere of Ipri, as well as the temperature range of Ipri, could have been used in the method of Chen et al., since Ipri teaches that a high quality dielectric of a TFT can

be formed by the high pressure oxidation performed in steam at temperatures in the range of 580 to 620°C" (emphasis added, pp. 3-4, Paper No. 30). The Applicants respectfully disagree.

First, it is noted that the test for obviousness is not whether the references "could have been" combined or modified as asserted in the Official Action, but rather whether the references should have been. As noted in MPEP § 2143.01, "The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination." *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990) (emphasis in original). Thus, it is respectfully submitted that the standard set forth in the Official Action is improper to support a finding of *prima facie* obviousness.

Second, it is respectfully submitted that the alleged motivation to combine Ipri and Chen is improper. The Official Action appears to assert that since Ipri teaches a process that is conducted at a temperature between 580°C and 620°C and Chen teaches that his process should be performed below 825°C, it would be obvious to pick and choose various features of Ipri and incorporate them into Chen. It is respectfully submitted that such assertion, however, is insufficient to motivate one of skill in the art to combine the references to achieve the present invention. The mere fact that Chen expresses a temperature preference for his process below 825°C is insufficient to conclude that one of skill in the art would thus be motivated to look to any or all other processes that are conducted below this temperature (such as that of Ipri) and to pick and choose various elements of those processes to be incorporated into Chen.

Third, the assertion in the Official Action that "Ipri teaches that a high quality dielectric of a TFT can be formed by the high pressure oxidation performed in steam at temperatures in the range of 580 to 620°C" (emphasis added) is simply incorrect. Ipri teaches forming a high quality dielectric of a TFT "at a pressure of one atmosphere" (col. 2, lines 56-57) or, for example, "in a steam ambient at one atmosphere" (col. 2, line 68-col. 3, line 1). The Applicants respectfully submit that 1 atm is not a pressurized atmosphere, let alone a "high pressure," and that nothing in Ipri teaches or suggests raising the pressure of the atmosphere. As noted in the interview of March 4, 2002, and the response of March 26, 2002, it was argued that the then-amended independent

claims include the feature "oxidizing the crystallized semiconductor film ... at a pressure greater than 1 atmosphere up to 15 atmospheres." Also, in the Official Action of October 21, 2002, and the Official Action of April 4, 2003, the Examiner recognizes that Ipri uses a pressure of 1 atm.

It is unclear why, if Ipri teaches a process by which a high quality dielectric of a TFT can be formed as the Official Action asserts, one of skill in the art would look to Chen, let alone to the combination of Ipri and Chen. More specifically, if one of skill in the art is merely looking to form a high quality dielectric, one need look no further than Ipri itself for a suitable method to form such dielectric. The apparent motivation asserted in the Official Action of a low temperature process is met by Ipri and the Official Action admits Ipri forms a suitable dielectric. Thus, it is respectfully submitted that one of skill in the art would not have been motivated to combine and modify Ipri and Chen, but would instead simply have practiced Ipri.

It is not clear why one with ordinary skill in the art would be motivated to combine the one atmosphere process of Ipri with the HiPOX process of Chen, and then also modify Chen to apply that combined process to a different part of the Chen device, that is the silicon region 3. There is no suggestion or motivation to apply the Chen HiPOX process used to densify layer 115 to the silicon region 3. Rather, the HiPOX process in Chen appears to be applied only to layers 111, 113 and 115, and not to silicon region 3 having source/drain regions 5 and channel region 7.

Still further, there is no suggestion or motivation to combine the process in Chen, where oxidation occurs after crystallization, with the process in Ipri, where oxidation and crystallization are performed simultaneously. Ipri discloses that amorphous silicon (i.e., a-Si) islands are initially deposited on the substrate and then simultaneously performs the oxidation and crystallization (col. 1, lines 60-68; col. 2, lines 1-60; Figs. 1-4). By doing this, the a-Si on the surface of the island is oxidized which does not meet the limitation of the instant independent claims requiring "oxidizing the crystallized semiconductor film" since the oxidation step is performed on the a-Si film. Further, the Official Action has provided no argument or documentation that such oxidation (of crystallized) silicon does inherently take place in the process of Ipri.

Troxell, Wolf I and Wolf II do not cure the deficiencies in Chen and Ipri. The Official Action relies on Troxell, Wolf I and Wolf II to allegedly teach an alkali-free glass substrate (p. 4, Paper No. 30), a pyrogenic oxidation step (p. 5, *Id.*), and a plasma CVD process (p. 7, *Id.*). Chen, Ipri, Troxell, Wolf I and Wolf II, either alone or in combination, do not provide a suggestion or motivation to combine the HiPOX process (5-10 atm) of layers 111, 113 and 115 of Chen with the low pressure process (1 atm) of Ipri and apply the combined process to silicon region 3 of Chen; to combine the process in Chen, which does not occur in a steam ambient, with the process in Ipri, which occurs in a 100% steam ambient; and to combine the process in Chen, where oxidation occurs after crystallization, with the process in Ipri, where oxidation and crystallization are performed simultaneously.

In the present application, it is respectfully submitted that the prior art of record, alone or in combination, does not expressly or impliedly suggest the claimed invention and the Official Action has not presented a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references.

For the reasons stated above, the Official Action has not formed a proper *prima facie* case of obviousness. Accordingly, reconsideration and withdrawal of the rejection under 35 U.S.C. § 103(a) are in order and respectfully requested.

B. Whether claims 1-105 do not conflict with claims 1, 2, 12, 13, 17 and 18 of copending Application No. 09/222,185, and with claims 1 and 6 of copending Application No. 09/615,078; and whether claims 1-105 are patentable under the doctrine of obviousness-type double patenting over claims 1-26 of the '185 application in view of U.S. Patent No. 5,275,851 to Fonash et al., and over claims 1-44 of the '078 application in view of Fonash.

The Official Action asserts that claims 1-105 of the present application conflict with claims 1, 2, 12, 13, 17 and 18 of copending Application No. 09/222,185, and with claims 1 and 6 of copending Application No. 09/615,078. The Official Action also provisionally rejects claims 1-105 under the doctrine of obviousness-type double

patenting over claims 1-26 of the '185 application in view of U.S. Patent No. 5,275,851 to Fonash et al., and over claims 1-44 of the '078 application in view of Fonash.

As stated in MPEP § 804, under the heading "Obviousness-Type," in order to form an obviousness-type double patenting rejection, a claim in the present application must define an invention that is merely an obvious variation of an invention claimed in the prior art patent, and the claimed subject matter must not be patentably distinct from the subject matter claimed in a commonly owned patent. Also, the patent principally underlying the double patenting rejection is not considered prior art.

The Applicants respectfully traverse the obviousness-type double patenting rejections because the independent claims of the present invention are patentably distinct from the claims of either the '185 application or the '078 application, either alone or in combination with Fonash.

All of the independent claims of the present invention recite oxidizing a crystallized semiconductor film to be active layers of thin film transistors. The claims of the '185 and '078 applications do not teach or suggest this feature. Fonash does not cure the deficiencies in the '185 and '078 applications. Fonash is relied upon to teach a catalyst. Therefore, the claims of the '185 and '078 applications, either alone or in combination with Fonash, do not teach or suggest oxidizing a crystallized semiconductor film to be active layers of thin film transistors.

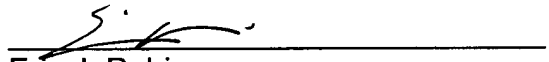
Also, independent claims 1, 17, 25, 41, 49, 63, 70 and 86 of the present invention recite a glass substrate and oxidizing a semiconductor film at a temperature lower than a strain point of the glass substrate. The claims of the '185 and '078 applications do not teach or suggest this feature. Again, Fonash does not cure the deficiencies in the '185 and '078 applications. Therefore, the claims of the '185 and '078 applications, either alone or in combination with Fonash, do not teach or suggest oxidizing a semiconductor film at a temperature lower than a strain point of a glass substrate.

Therefore, the Applicants respectfully submit that the subject application is patentably distinct from the claims of either the '185 application or the '078 application, either alone or in combination with Fonash. Reconsideration of the obviousness-type double patenting rejection is requested.

In any event, it is noted that the claims in the '185 and '078 applications may be amended after the filing of the present *Appeal Brief*. Therefore, the Applicants respectfully request that the assertion of conflicting claims and the double patenting rejections be held in abeyance until an indication of allowable subject matter is made in either the present application or the copending applications. At such time, the Applicants will respond to any remaining conflicts and/or double patenting rejections.

The present application is believed to be in condition for allowance and favorable reconsideration is respectfully requested. If the Examiner feels further discussions would expedite prosecution of this application, he is invited to contact the undersigned.

Respectfully submitted,



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IX. APPENDICES

A. Claims involved in the appeal.

B. U.S. Patent No. 5,322,807 to Chen et al.

C. U.S. Patent No. 4,597,160 to Ipri.

D. U.S. Patent No. 4,851,363 to Troxell et al.

E. Wolf et al., "Silicon Processing for the VLSI Era, Volume 1: Process Technology," 1986, pp. 171-175.

F. Wolf et al., "Silicon Processing for the VLSI Era, Volume 1: Process Technology," 1986, pp. 216-218.

G. The pending claims of copending Application No. 09/222,185.

H. The pending claims of copending Application No. 09/615,078.

I. U.S. Patent No. 5,275,851 to Fonash et al.

APPENDIX A

PENDING CLAIMS

1. A method of manufacturing a semiconductor device having a plurality of thin film transistors, comprising the steps of:

forming a semiconductor film comprising silicon over a glass substrate;

crystallizing said semiconductor film; and

oxidizing the crystallized semiconductor film to be active layers of said thin film transistors in a pressurized atmosphere at a pressure greater than one atmosphere upto 15 atmospheres and at a temperature lower than a strain point of said glass substrate.

2. (Canceled)

3. A method according to claim 1, wherein said oxidizing is performed in an oxidizing atmosphere.

4. A method according to claim 1, wherein said oxidizing is performed in an oxidizing atmosphere containing water vapor.

5. A method according to claim 1, wherein said temperature is in a range of 500 to 650°C.

6. A method according to claim 1, wherein said semiconductor film has a thickness of 100 to 1,000 Å.

7. A method according to claim 1, wherein at least one region of the semiconductor film is completely oxidized to a bottom surface of the semiconductor film during said oxidizing step.

8. A method according to claim 1, wherein said semiconductor device comprises an active matrix type display device.

9. A method of manufacturing a semiconductor device having a plurality of thin film transistors, comprising the steps of:

forming a semiconductor film comprising silicon on an insulating surface;

crystallizing said semiconductor film; and

oxidizing the crystallized semiconductor film to be active layers of said thin film transistors in a pressurized atmosphere at a pressure greater than one atmosphere upto 15 atmospheres and at a temperature of 500 to 650°C.

10. (Canceled)

11. A method according to claim 9, wherein said oxidizing is performed in an oxidizing atmosphere.

12. A method according to claim 9, wherein said oxidizing is performed in an oxidizing atmosphere containing water vapor.

13. A method according to claim 9, wherein said oxidizing step is a pyrogenic oxidation process.

14. A method according to claim 9, wherein said semiconductor film has a thickness of 100 to 1,000 Å.

15. A method according to claim 9, wherein at least one region of the semiconductor film is completely oxidized to a bottom surface of the semiconductor film during said oxidizing step.

16. A method according to claim 9, wherein said semiconductor device comprises an active matrix type display device.

17. A method of manufacturing a semiconductor device having a plurality of thin film transistors, comprising the steps of:

forming a semiconductor film comprising silicon over an alkali-free glass substrate;

crystallizing said semiconductor film; and

oxidizing the crystallized semiconductor film to be active layers of said thin film transistors in a pressurized atmosphere at a pressure greater than one atmosphere

upto 15 atmospheres and at a temperature lower than a strain point of said glass substrate.

18. (Canceled)

19. A method according to claim 17, wherein said oxidizing is performed in an oxidizing atmosphere.

20. A method according to claim 17, wherein said oxidizing is performed in an oxidizing atmosphere containing water vapor.

21. A method according to claim 17, wherein said temperature is in a range of 500 to 650°C.

22. A method according to claim 17, wherein said semiconductor film has a thickness of 100 to 1,000 Å.

23. A method according to claim 17, wherein at least one region of the semiconductor film is completely oxidized to a bottom surface of the semiconductor film during said oxidizing step.

24. A method according to claim 17, wherein said semiconductor device comprises an active matrix type display device.

25. A method of manufacturing a semiconductor device having a plurality of thin film transistors, comprising the steps of:

forming a semiconductor film comprising silicon over a glass substrate;

crystallizing said semiconductor film;

forming an insulating film adjacent to said crystallized semiconductor film by plasma CVD; and

forming gate electrodes adjacent to said insulating film,

wherein said method further comprises a step of oxidizing the crystallized semiconductor film to be active layers of said thin film transistors in a pressurized atmosphere at a pressure greater than one atmosphere upto 15 atmospheres and at a temperature lower than a strain point of said glass substrate.

26. (Canceled)

27. A method according to claim 25, wherein said gate electrodes are formed over said active layers.

28. A method according to claim 25, wherein said oxidizing is performed in an oxidizing atmosphere containing water vapor.

29. A method according to claim 25, wherein said temperature is in a range of 500 to 650°C.

30. A method according to claim 25, wherein said semiconductor film has a thickness of 100 to 1,000 Å.

31. A method according to claim 25, wherein at least one region of the semiconductor film is completely oxidized to a bottom surface of the semiconductor film during said oxidizing step.

32. A method according to claim 25, wherein said semiconductor device comprises an active matrix type display device.

33. A method of manufacturing a semiconductor device having a plurality of thin film transistors, comprising the steps of:

forming a semiconductor film comprising silicon on an insulating surface;

crystallizing said semiconductor film;

forming an insulating film adjacent to said crystallized semiconductor film by plasma CVD; and

forming gate electrodes adjacent to said insulating film,

wherein said method further comprises a step of oxidizing the crystallized semiconductor film to be active layers of said thin film transistors in a pressurized atmosphere at a pressure greater than one atmosphere upto 15 atmospheres and at a temperature of 500 to 650°C.

34. (Canceled)

35. A method according to claim 33, wherein said gate electrodes are formed over said active layers.

36. A method according to claim 33, wherein said oxidizing is performed in an oxidizing atmosphere containing water vapor.

37. A method according to claim 33, wherein said oxidizing step is a pyrogenic oxidation process.

38. A method according to claim 33, wherein said semiconductor film has a thickness of 100 to 1,000 Å.

39. A method according to claim 33, wherein at least one region of the semiconductor film is completely oxidized to a bottom surface of the semiconductor film during said oxidizing step.

40. A method according to claim 33, wherein said semiconductor device comprises an active matrix type display device.

41. A method of manufacturing a semiconductor device having a plurality of thin film transistors, comprising the steps of:

forming a semiconductor film comprising silicon over an alkali-free glass substrate;

crystallizing said semiconductor film;

forming an insulating film adjacent to said crystallized semiconductor film by plasma CVD; and

forming gate electrodes adjacent to said insulating film,

wherein said method further comprises a step of oxidizing the crystallized semiconductor film to be active layers of said thin film transistors in a pressurized atmosphere at a temperature lower than a strain point of said glass substrate.

42. (Canceled)

43. A method according to claim 41, wherein said gate electrodes are formed over said active layers.

44. A method according to claim 41, wherein said oxidizing is performed in an oxidizing atmosphere containing water vapor.

45. A method according to claim 41, wherein said temperature is in a range of 500 to 650°C.

46. A method according to claim 41, wherein said semiconductor film has a thickness of 100 to 1,000 Å.

47. A method according to claim 41, wherein at least one region of the semiconductor film is completely oxidized to a bottom surface of the semiconductor film during said oxidizing step.

48. A method according to claim 41, wherein said semiconductor device comprises an active matrix type display device.

49. A method of manufacturing a semiconductor device having a plurality of thin film transistors, comprising the steps of:

forming a semiconductor film comprising silicon over a glass substrate;

crystallizing said semiconductor film; and

oxidizing the crystallized semiconductor film to be active layers of said thin film transistors in a pressurized atmosphere at a pressure greater than one atmosphere upto 15 atmospheres; and

wherein said oxidizing the semiconductor film is performed in a temperature lower than a strain point of said glass substrate.

50. A method according to claim 49, wherein said strain point of said substrate is 750°C or less.

51. A method according to claim 49, wherein said oxidizing atmosphere contains water vapor.

52. A method according to claim 49, wherein said temperature is in a range of 500 to 650°C.

53. A method according to claim 49, wherein said semiconductor film has a thickness of 100 to 1,000 Å.

54. A method according to claim 49, wherein at least one region of the semiconductor film is completely oxidized to a bottom surface of the semiconductor film during said heating step.

55. A method according to claim 49, wherein said semiconductor device comprises an active matrix type display device.

56. A method of manufacturing a semiconductor device having a plurality of thin film transistors, comprising the steps of:

forming a semiconductor film comprising silicon on an insulating surface;

crystallizing said semiconductor film; and

oxidizing the crystallized semiconductor film to be active layers of said thin film transistors in a pressurized atmosphere at a pressure greater than one atmosphere upto 15 atmospheres; and

wherein said oxidizing the semiconductor film is performed in a temperature of 500 to 650°C.

57. A method according to claim 56, wherein said crystallizing step is performed at a temperature of 600°C.

58. A method according to claim 56, wherein said oxidizing atmosphere contains water vapor.

59. A method according to claim 56, wherein said oxidizing step is a pyrogenic oxidation process.

60. A method according to claim 56, wherein said semiconductor film has a thickness of 100 to 1,000 Å.

61. A method according to claim 56, wherein at least one region of the semiconductor film is completely oxidized to a bottom surface of the semiconductor film during said heating step.

62. A method according to claim 56, wherein said semiconductor device comprises an active matrix type display device.

63. A method of manufacturing a semiconductor device having a plurality of thin film transistors, comprising the steps of:

forming a semiconductor film comprising silicon over an alkali-free glass substrate;

crystallizing said semiconductor film; and

oxidizing the crystallized semiconductor film to be active layers of said thin film transistors in pressurized atmosphere at a pressure greater than one atmosphere upto 15 atmospheres; and, for electrically isolating said plurality of thin film transistors from one another,

wherein said oxidizing the semiconductor film is performed in a temperature lower than a strain point of said glass substrate.

64. A method according to claim 63, wherein said strain point of said substrate is 750°C or less.

65. A method according to claim 63, wherein said oxidizing atmosphere contains water vapor.

66. A method according to claim 63, wherein said temperature is in a range of 500 to 650°C.

67. A method according to claim 63, wherein said semiconductor film has a thickness of 100 to 1,000 Å.

68. A method according to claim 63, wherein at least one region of the semiconductor film is completely oxidized to a bottom surface of the semiconductor film during said heating step.

69. A method according to claim 63, wherein said semiconductor device comprises an active matrix type display device.

70. A method of manufacturing a semiconductor device having a plurality of thin film transistors, comprising the steps of:

forming a semiconductor film comprising silicon over a glass substrate;

crystallizing said semiconductor film;

forming an insulating film adjacent to said crystallized semiconductor film; and

forming gate electrodes adjacent to said insulating film,

wherein said method further comprises a step of oxidizing the crystallized semiconductor film to be active layers of said thin film transistors in a pressurized atmosphere at a pressure greater than one atmosphere upto 15 atmospheres; and

wherein said oxidizing the semiconductor film is performed in a temperature lower than a strain point of said glass substrate.

71. A method according to claim 70, wherein said strain point of said substrate is 750°C or less.

72. A method according to claim 70, wherein said gate electrodes are formed over said active layers.

73. A method according to claim 70, wherein said oxidizing atmosphere contains water vapor.

74. A method according to claim 70, wherein said temperature is in a range of 500 to 650°C.

75. A method according to claim 70, wherein said semiconductor film has a thickness of 100 to 1,000 Å.

76. A method according to claim 70, wherein at least one region of the semiconductor film is completely oxidized to a bottom surface of the semiconductor film during said oxidizing step.

77. A method according to claim 70, wherein said semiconductor device comprises an active matrix type display device.

78. A method of manufacturing a semiconductor device having a plurality of thin film transistors, comprising the steps of:

forming a semiconductor film comprising silicon on an insulating surface;

crystallizing said semiconductor film;

forming an insulating film adjacent to said crystallized semiconductor film; and

forming gate electrodes adjacent to said insulating film,

wherein said method further comprises a step of oxidizing the crystallized semiconductor film to be active layers of said thin film transistors in a pressurized atmosphere at a pressure greater than one atmosphere upto 15 atmospheres; and

wherein said oxidizing the semiconductor film is performed in a temperature of 500 to 650°C.

79. A method according to claim 78, wherein said crystallizing step is performed at a temperature of 600°C.

80. A method according to claim 78, wherein said gate electrodes are formed over said active layers.

81. A method according to claim 78, wherein said oxidizing atmosphere contains water vapor.

82. A method according to claim 78, wherein said oxidizing step is a pyrogenic oxidation process.

83. A method according to claim 78, wherein said semiconductor film has a thickness of 100 to 1,000 Å.

84. A method according to claim 78, wherein at least one region of the semiconductor film is completely oxidized to a bottom surface of the semiconductor film during said oxidizing step.

85. A method according to claim 78, wherein said semiconductor device comprises an active matrix type display device.

86. A method of manufacturing a semiconductor device having a plurality of thin film transistors, comprising the steps of:

forming a semiconductor film comprising silicon over an alkali-free glass substrate;

crystallizing said semiconductor film;

forming an insulating film adjacent to said crystallized semiconductor film; and

forming gate electrodes adjacent to said insulating film,

wherein said method further comprises a step of oxidizing the crystallized semiconductor film to be active layers of said thin film transistors in a pressurized atmosphere at a pressure greater than one atmosphere upto 15 atmospheres; and

wherein said oxidizing the semiconductor film is performed in a temperature lower than a strain point of said glass substrate.

87. A method according to claim 86, wherein said strain point of said substrate is 750°C or less.

88. A method according to claim 86, wherein said gate electrodes are formed over said active layers.

89. A method according to claim 86, wherein said oxidizing atmosphere contains water vapor.

90. A method according to claim 86, wherein said temperature is in a range of 500 to 650°C.

91. A method according to claim 86, wherein said semiconductor film has a thickness of 100 to 1,000 Å.

92. A method according to claim 86, wherein at least one region of the semiconductor film is completely oxidized to a bottom surface of the semiconductor film during said oxidizing step.

93. A method according to claim 86, wherein said semiconductor device comprises an active matrix type display device.

94. A method according to claim 1, wherein said strain point of said substrate is 750°C or less.

95. A method according to claim 17, wherein said strain point of said substrate is 750°C or less.

96. A method according to claim 25, wherein said strain point of said substrate is 750°C or less.

97. A method according to claim 41, wherein said strain point of said substrate is 750°C or less.

98. A method according to claim 1, wherein said oxidizing step is a pyrogenic oxidation process.

99. A method according to claim 17, wherein said oxidizing step is a pyrogenic oxidation process.

100. A method according to claim 25, wherein said oxidizing step is a pyrogenic oxidation process.

101. A method according to claim 41, wherein said oxidizing step is a pyrogenic oxidation process.

102. A method according to claim 49, wherein said oxidizing step is a pyrogenic oxidation process.

103. A method according to claim 63, wherein said oxidizing step is a pyrogenic oxidation process.

104. A method according to claim 70, wherein said oxidizing step is a pyrogenic oxidation process.

105. A method according to claim 86, wherein said oxidizing step is a pyrogenic oxidation process.

106. A method according to claim 1, wherein an exposed surface of said crystallized semiconductor film is oxidized by said oxidizing.

107. A method according to claim 9, wherein an exposed surface of said crystallized semiconductor film is oxidized by said oxidizing.

108. A method according to claim 17, wherein an exposed surface of said crystallized semiconductor film is oxidized by said oxidizing.

109. A method according to claim 25, wherein an exposed surface of said crystallized semiconductor film is oxidized by said oxidizing.

110. A method according to claim 33, wherein an exposed surface of said crystallized semiconductor film is oxidized by said oxidizing.

111. A method according to claim 41, wherein an exposed surface of said crystallized semiconductor film is oxidized by said oxidizing.

112. A method according to claim 49, wherein an exposed surface of said crystallized semiconductor film is oxidized by said oxidizing.

113. A method according to claim 56, wherein an exposed surface of said crystallized semiconductor film is oxidized by said oxidizing.

114. A method according to claim 63, wherein an exposed surface of said crystallized semiconductor film is oxidized by said oxidizing.

115. A method according to claim 70, wherein an exposed surface of said crystallized semiconductor film is oxidized by said oxidizing.

116. A method according to claim 78, wherein an exposed surface of said crystallized semiconductor film is oxidized by said oxidizing.

117. A method according to claim 86, wherein an exposed surface of said crystallized semiconductor film is oxidized by said oxidizing.